IMPEDANCE-CONTROLLED WRITE DRIVER FOR LOW POWER PREAMP

TECHNICAL FIELD

[001] The invention relates to hard disk drive assemblies. More particularly, the invention relates to methods and apparatus for impedance control in write head driver circuitry.

BACKGROUND OF THE INVENTION

[002] For high performance hard disk drive assemblies, very fast rising and falling times and precise impedance control are required in order to maximize the performance of write drivers. Low power supply voltage is generally preferred to avoid potential problems with excessive power consumption and heat dissipation. Conventional series-type impedance control circuits have problems including, but not limited to, power supply voltage, or "headroom" degradation due to a voltage drop over matching resistors placed in series. In addition, write current tolerance is limited by the inevitable variation in the impedance of internal series resistors.

[003] Another challenge faced by series-connected impedance control circuits known in the arts is their response to changes in the write current. The write current naturally tends to be dependent upon the write head impedance. Referring to the representative prior art circuit shown in Figure 1, write current I_W that flows into the write head is determined by the ratio of the internal reference resistance R_o and the external write-head-impedance ($R_h + R_{fpc}$). Because of this, write-current is dependent on not only the inherent variations present in the internal resistance, but also on the write-head-impedance.

Increasing the internal reference resistor R_o decreases the write current's dependency on the write-head-impedance, but detrimentally increases the voltage V_h drop across the write head.

[004] Swing voltage asymmetry is another problem faced by write driver circuits known in the arts. Asymmetric swings in head voltage can result in loss of stored data and damage to the heads. Typically between a preamp and a recording head (i.e. write head), and a reading head (not shown) there are wires or lines for both writing and reading. Due to area constraints, the lines are typically closely spaced, e.g. on the order of about 50-100um, making them susceptible to "write-to-read coupling" or "crosstalk" resulting from mutual interference. The swing voltage of the write lines can be very fast and large in magnitude, sometimes causing damage to the heads through capacitive and/or inductive coupling between the write lines and read lines.

[005] These and other problems encountered by prior art conventional write driver circuitry, such as that represented by the example shown in Figure 1, make it difficult to provide both current-accuracy and high-performance while also using a low voltage power supply. It would be useful and desirable in the arts to provide improved impedance-controlled write driver apparatus and methods. It would be advantageous to provide a reliable and accurate impedance-controlled write driver circuit for use with a low voltage power supply. Advantages would also be obtained by avoiding the reduction of headroom and making head voltage swings symmetrical.

SUMMARY OF THE INVENTION

[006] In carrying out the principles of the present invention, in accordance with preferred embodiments thereof, methods and apparatus are provided for impedance-controlled write drivers.

[007] According to one aspect of the invention, a method of coupling a magnetic read/write head to a driver current source is provided. Steps include coupling a read/write head to a flexible printed circuit containing read lines and write lines. The flexible printed circuit has two opposing terminals wherein each is coupled to one of two approximately matched impedance control circuits in parallel with the current source.

[008] According to another aspect of the invention, a method of coupling a read/write head to a driver circuit also includes a further step of linking the opposing flexible printed circuit terminals with a capacitor in order to minimize DC current loss.

[009] According to yet another aspect of the invention, an impedance-controlled write driver circuit is provided, in which a write head is operably coupled to a flexible printed circuit having two opposing terminals for external coupling. Each of a symmetrical pair of matched impedance control circuits is coupled between an opposing terminal of the flexible printed circuit and a write driver circuit ground.

[010] According to still another aspect of the invention, an impedance-controlled write driver circuit is configured such that the head voltage V_h may be described

by the formula, $V_h = I_W * (R_h + R_{fpc} + R_o) \div (R_h + R_{fpc})$, wherein: I_W represents a write head current; R_h represents a write head resistance; R_{fpc} represents the resistance of the flexible printed circuit; and R_o represents a selected internal reference resistance.

[012] Preferred embodiments of the invention are described in which an impedance-controlled write driver circuit includes two matched impedance control circuits, each having a resistance value of about $R_o/2$.

[013] The invention provides technical advantages including but not limited to providing accurate and operation without a reduction in the headroom of the write driver. The AC-coupled impedance control circuit of the invention does not influence the DC write current, so the write current is determined solely by the current source setting. The symmetrical circuit configuration provides a symmetrical head voltage swing, which minimizes damage to MR heads in the event of the application of excess voltage. These and other features, advantages, and benefits of the present invention will become apparent to one of ordinary skill in the art upon careful consideration of the detailed description of representative embodiments of the invention in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[014] The present invention will be more clearly understood from consideration of the following detailed description and drawings in which:

[015] Figure 1 (prior art) is a schematic block diagram showing an example of a write driver architecture known in the arts;

[016] Figure 2 is a schematic block diagram showing an example of a preferred embodiment of the invention;

[017] Figure 3 is a schematic block diagram showing an example of an alternative preferred embodiment of the invention;

[018] Figure 4 is a schematic block diagram showing an example of another alternative preferred embodiment of the invention;

[019] Figure 5 is a schematic block diagram showing an example of another alternative preferred embodiment of the invention; and

[020] Figure 6 is a schematic block diagram showing an example of another alternative preferred embodiment of the invention.

[021] References in the detailed description correspond to like references in the figures unless otherwise noted. Like numerals refer to like parts throughout the various figures. Descriptive and directional terms used in the written description such as first, second, left, right, etc., refer to the drawings themselves as laid out on the paper and not to physical limitations of the invention unless specifically noted. The drawings are not to scale, and some features of embodiments shown and discussed may be simplified or amplified for illustrating the principles, features, and advantages of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[022] An example of the impedance control circuit architecture for implementing the invention is shown in Figure 2. In this preferred embodiment, impedance control circuitry 20 is shown. The write head 22 is connected to associated preamp circuitry 24 via a flexible printed circuit 26 including two write lines. Data input ports, typically transistors represented by Q1, Q2, Q3, and Q4, are provided for switching writing functions at the head 22 as familiar to those skilled in the arts. The impedance control circuitry 20 is preferably included as a portion of the preamp 24 circuitry. It should be understood that the impedance control circuitry 20 is seen in parallel from the point of view of the head 22.

[023] Various configurations of impedance control circuitry 20 may be used within the concept and principles of the architecture of the invention, the methods and apparatus of which is represented in Figure 2. According to the preferred embodiments of the invention, as long as the configuration of the impedance control circuitry 20 ensures that symmetry is maintained between the swing voltages of the lines of the FPC 26, the voltage of each write line is maintained as the polar opposite of that of the read line at any given moment. In this way the potential for damage to the head 22 by voltage swings is minimized or altogether avoided. Additionally, the parallel impedance control circuit 20 configuration significantly avoids reduction of the headroom of the driver circuit 24.

[024] The write driver circuit referred to in Figure 2 is shown in an implementation wherein each of two matched impedance control circuits 20 is

provided in a configuration including a resistor 28 having a resistance value of about $R_0/2$ relative to the internal reference resistance R_0 of the write head 22. The resistors 28 are preferably matched in resistance value as closely as feasible and are electrically coupled respectively between nodes A and B of Figure 2 and ground. Thus, the relationship of the write head 22 voltage H_V to the write current W_I may be described by the relationship, $V_h = I_W * (R_h + R_{fpc} + R_o) \div (R_h + R_{fpc})$. Although variations in the arrangement of the circuit are possible, a circuit topology described by this equation will not depart from the principles of the invention.

[025] Now referring primarily to Figure 3, a schematic diagram of an example of an alternative preferred embodiment of a write driver circuit 24 with an impedance control circuit 30 according to the invention is depicted. In this alternative embodiment, for each of the matched circuits 30, a first resistor 32 having a resistance value of about $R_o/2$ is electrically coupled to the first terminal of a capacitor 34. The second terminal of the capacitor 34 is coupled to a second resistor 36. The second resistor 36 has a resistance value of approximately $R_{dc}/2$, where R_{dc} represents the DC resistance of the write head 22. The second terminal of the capacitor 34 is coupled to ground. Each of the impedance control circuits 30, with components preferably matched as closely as feasible, is coupled respectively to nodes A and B.

[026] With reference primarily to Figure 4, a schematic diagram of an example of another alternative preferred embodiment of an impedance control circuit 40 according to the invention is shown. In this alternative configuration 40 an electrical path 42 between the two FPC terminals A and B is provided. In this

path 42, a first resistor 44, having a resistance value of about R_o, is connected in series with a capacitor 46. Of course these components 44, 46 could be reversed from the configuration shown 40 without departure from the invention. A second resistor 48 preferably having a resistance value of about $R_{dc}/2$ is electrically coupled between each of nodes A and B and ground. As with the other alternative embodiments, the second resistors 48 are preferably matched as closely as feasible in terms of resistance values.

[027] An additional alternative embodiment of a write driver circuit 24 using an impedance control circuit 50 according to the invention is shown in Figure 5. As shown, in this additional alternative configuration 50 an electrical path 52 between the two FPC terminals A and B is provided. In this path 52, a first resistor 54, having a resistance value of about R_o, is connected in series with a capacitor 56. As shown, a switch 57 may be placed between the first resistor 54 and the capacitor 56. This switch 57 is preferably placed in the "on" position to allow the first resistor 54 and capacitor 56 to set impedance matching. The switch 57 is preferably placed in the "off" position when the voltage is in transition, i.e., from high to low, or from low to high, allowing faster rise times. A second resistor 58 preferably having a resistance value of about $R_{dc}/2$ is electrically coupled between each of nodes A and B and ground. As with the other alternative embodiments, the second resistors 58 are preferably matched as closely as feasible in terms of resistance values.

[028] An alternative embodiment shown in Figure 6 illustrates a schematic diagram of an example of another alternative preferred embodiment of an impedance control circuit 60 according to the invention. A first resistor 62 is

coupled between nodes A and B and the opposing terminals of a capacitor 64. The resistors 62 preferably each have a resistance value of about $R_o/2$, and are as closely matched as feasible. Coupled between the junction of each resistor 62 with the respective terminals of the capacitor 64 and ground, matching diodes 66 are provided as shown.

[029] Thus, the invention provides impedance-controlled write driver circuits and methods for low-power applications in which there is not significant headroom loss due to mismatching resistors. The invention also ensures that write head impedance is independent of write current, and that head voltage swing symmetry is maintained. The symmetrical head voltage swing minimizes damage to MR heads in the event of the application of excess voltage. While the invention has been described with reference to certain illustrative embodiments, the description of the methods and devices described are not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments as well as other advantages and embodiments of the invention will be apparent to persons skilled in the art upon reference to the description and claims.